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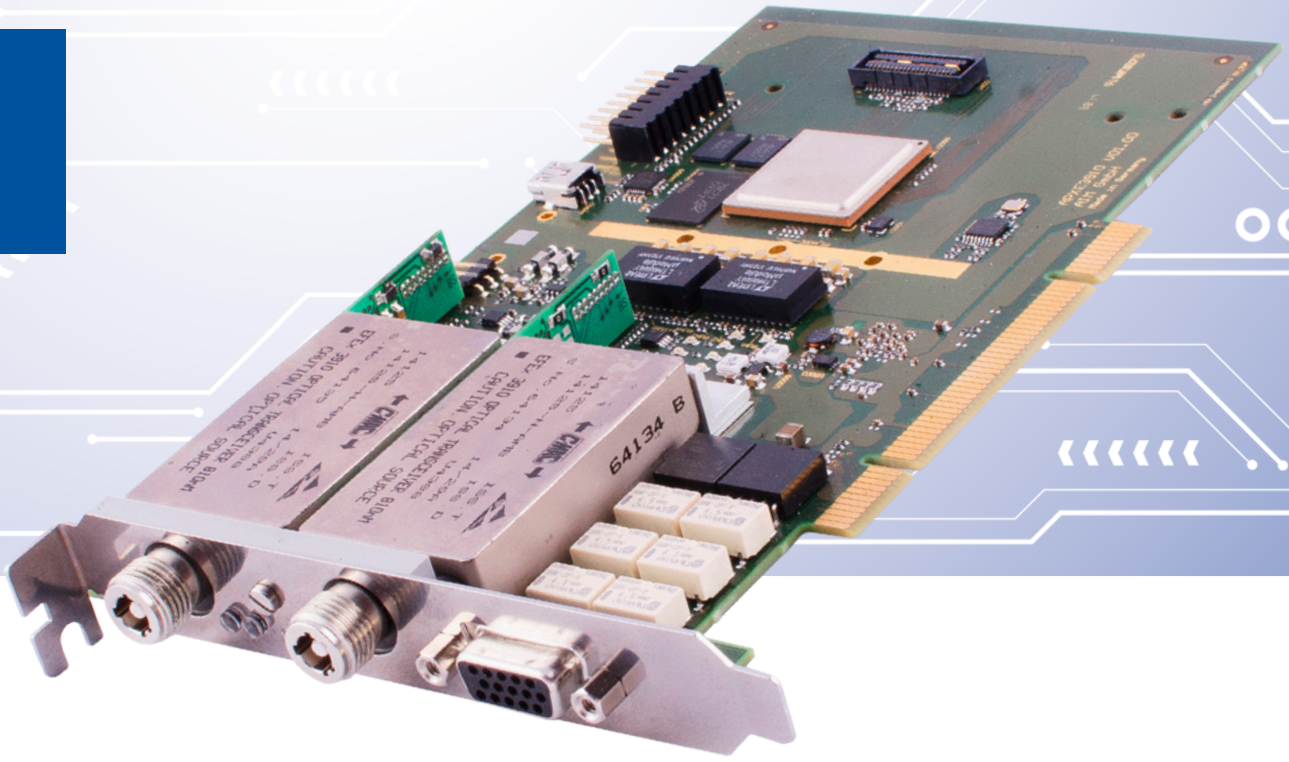
APXX3910

Single Stream STANAG3910/EFEX Test & Simulation Module for PCI

Data Sheet



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APXX3910

Single Stream STANAG3910/EFEX Test & Simulation Module for PCI

General Features

The ► **APXX3910** is a member of AIM's latest family of PCI modules for analysing, simulating, monitoring and testing of ► **STANAG3910/EFAbus Express (EFEX)** databuses. The APXX3910 module concurrently acts as the Bus Controller, Multiple Remote Terminals (31) and Chronological/ Mailbox Bus Monitor.
The APXX3910 provides 1 fully independent dual redundant STANAG3910 high speed and low speed interface on a short length PCI card form factor.
The APXX3910 can be used for protocol testing and simulation of STANAG3910 LS/HS Bus Controller, Multiple Remote Terminals and Chronological Monitoring at full bus loads.

All BC/RT/BM operations are performed concurrently with no degradation of performance in any operational LS/HS mode. The HS section of the APXX3910 supports EFAbus Direct Digital Links (DDL) and Fibre Optic DDL (FODDL) acquisition. EFAbus Express (EFEX) extensions to the STANAG3910 protocol are fully supported and both protocols are co-resident and accessible by a software switch.

The APXX3910 incorporates full protocol error injection and detection and allows the reconstruction and replay of previously recorded electrical/optical STANAG3910 bus traffic to the LS/HS databus with excellent timing accuracy. The APXX3910 provides a single PCI slot solution with all the databus electrical and optical signals accessible on a single front panel.

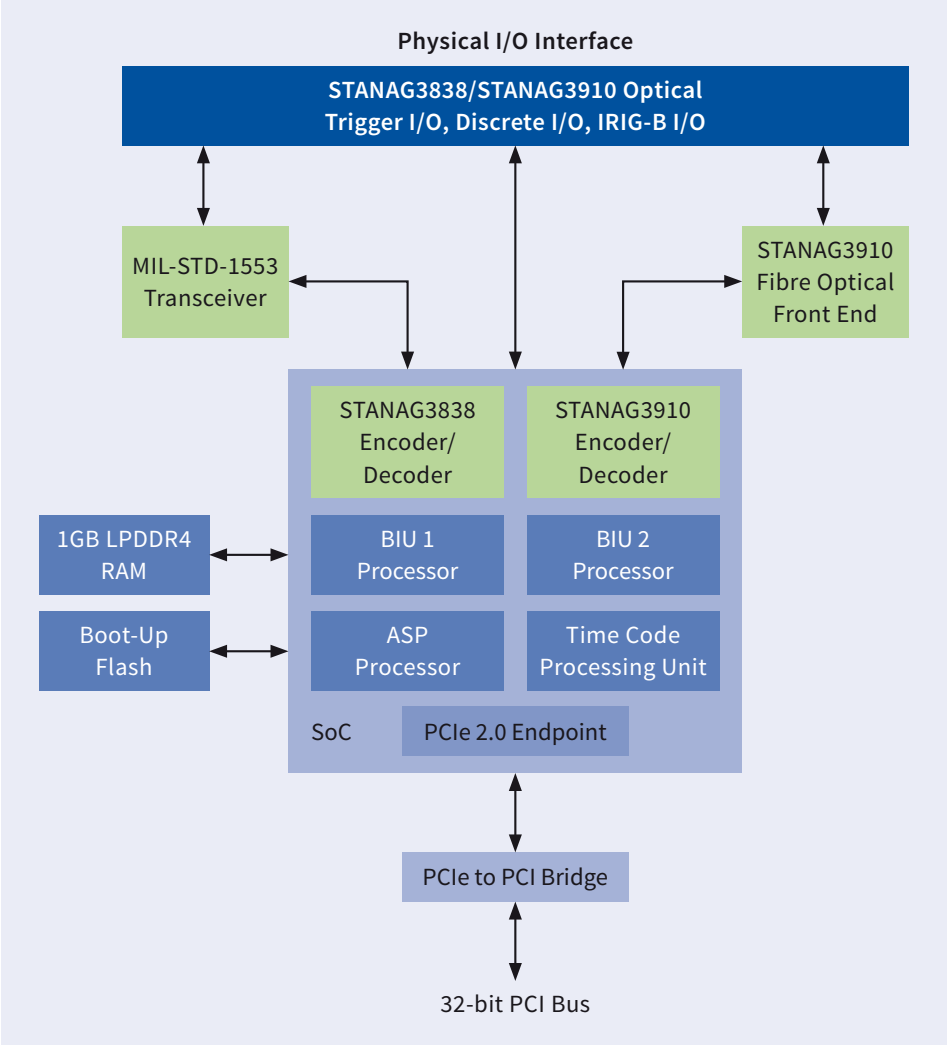
The APXX3910 card uses AIM's latest SoC (System-on-Chip) based hardware design with 2 dual core processing units.
One dual core section is implementing the STANAG3838 and STANAG3910 Bus Interface Units (BIUs). On the second dual core section the Application Support Processor (ASP) is implemented under Linux OS and executes the driver software onboard and minimizes the load on the host processing system. The onboard processing capabilities and a 1GB LPDDR4 RAM memory allows autonomous operation for real time applications and reduces interaction with the host processing system.

An IRIG-B time encoder/decoder that provides both sinusoidal and a free-wheeling mode is included for time tag synchronization at the system level for single or multiple APXX3910 modules. The card also includes 8 Open/Ground Avionics Level (+35V) discrete I/O signals.

Full function driver software is delivered with the APXX3910 card in comprehensive Board Software Packages (BSPs) for Windows and Linux.

The optional ► **PBA.pro™** databus test and analysis tool (for Windows and Linux) can also be purchased for use with the APXX3910 card.

APXX3910 Block Diagram



Bus Controller

The APXX3910 provides real time Bus Controller (BC) functions for the dual redundant STANAG3910 LS/HS databus system including data buffer queues for generation of dynamic data functions such as EFAbus Dynamic Tags for LS/HS messages.

Key Features of the Bus Controller Mode include:
- Autonomous operation including sequencing of LS Minor/Major Frames
- Acyclic Message Insertion/Deletion
- Programmable BC Retry without host Interaction
- Programmable HS Transmitter initialize Time and HS Receiver Timeout
- Full LS/HS Error Injection down to Word and Bit Level
- Supports EFAbus Message Multiplexing
- Multi-Buffering with Real Time Data Buffer Updates
- Synchronization of BC Operation to external Trigger Inputs
- LS Bus 4µs Intermessage Gaps

Multiple Remote Terminal

The APXX3910 can simulate up to 31 LS/HS Remote Terminals with all sub-addresses each providing individually programmable Response Time. Each HS RT simulates all 128 Message Identifiers (MID). LS/HS RT's can be programmed in Mailbox Monitor mode for non-simulated RT's.

The interface provides data buffer queues allowing the generation of dynamic data functions such as EFAbus dynamic tags for LS/HS messages.

Key Features of the Remote Terminal Simulation Mode include:
- Programmable Response Time for each RT with fast RT Response at 4µs
- Multi-Buffering for each simulated RT, Sub-Address and MID
- Full LS/HS Error Injection for each simulated RT, Sub-Address and MID down to Word and Bit level
- Programmable and Intelligent Response to Mode Codes
- Multi-Buffering with Real Time Data Buffer Updates
- Supports EFAbus Message Multiplexing

Chronological Bus Monitor

The APXX3910 includes a powerful LS/HS Chronological Bus Monitor and analysis function with multiple trigger and programmable capture capabilities. Accurate time tagging of both LS and HS messages, intermessage gaps, response time and transmitter initialize time is supported. LS/HS messages are time tagged to a 1µs resolution. LS response time and intermessage gaps as well as HS transmitter initialize time are measured down to 0.25µs.

Key Features of the Chronological Bus Monitor include:

Multi Level Complex Sequence Trigger on:
- LS/HS Error, LS/HS Word
- LS/HS Data Word in Limits

Monitor and Bus Traffic Capture:
- 1GByte of Onboard Memory for LS/HS Messages
- Trigger on Start, Centre and End
- LS/HS Message Counters

EFAbus Express (EFEX) Functionality

The APXX3910 module supports EFAbus Express (EFEX) protocol in all operating modes and at full bus rates.
EFEX functionality is co-resident with STANAG3910 protocol to support either Tranche I or Tranche II Typhoon aircraft standard. Selection of STANAG3910 or EFEX mode is via a software switch.

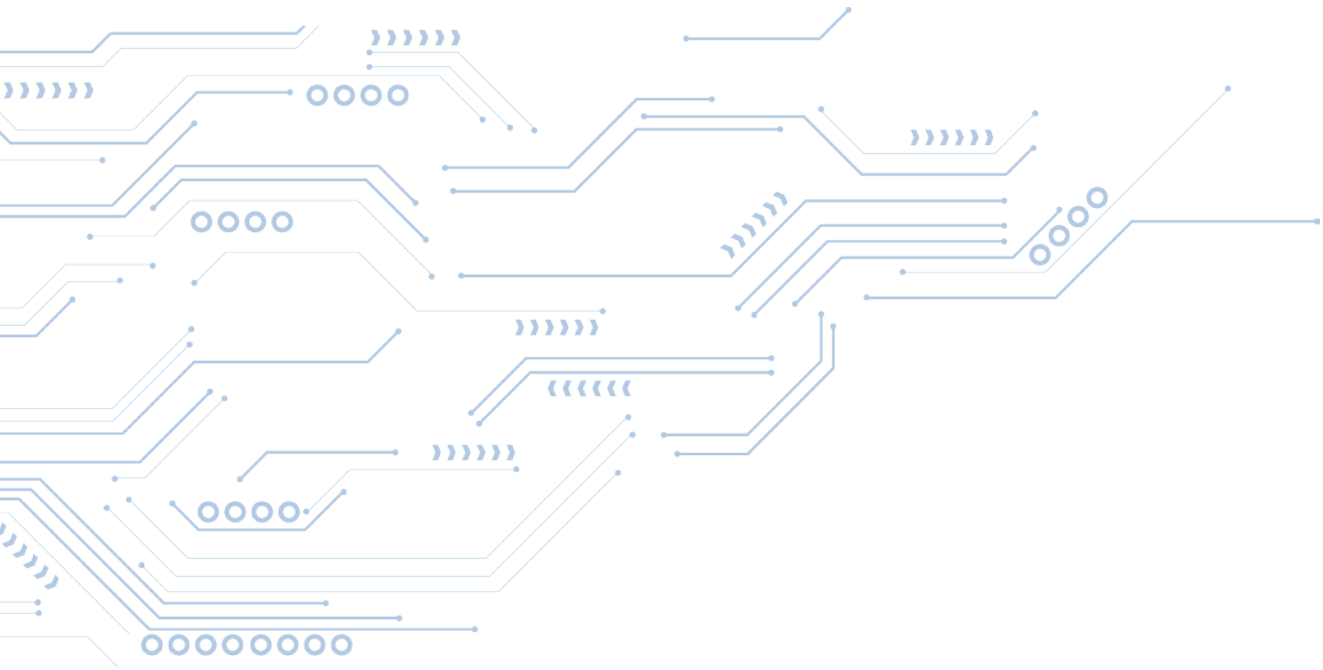
Key functions of the EFEX mode operation include:

EFEX Bus Control
- EFEX Bus Controller Simulation of all Transfer Types
- Control, Status and Status/Data Command Frame Control
- Simulation of Gap and Wait Time Setting Control
- EFEX Mode Code Support
- Error Injection/Detection
- EFEX Mixed Mode Simulation and Monitoring

EFEX RT Simulation
- EFA/EFEX Dual Mode RT Simulation for all EFEX BC Commands
- EFEX HS RT Response Time Setting Control for SD and S Frame
- HS Mode Code Simulation for EFEX RTs
- Error Injection

EFEX Bus Monitoring
- Chronological and Mailbox Bus Monitoring of EFEX Bus Traffic
- Capture and Decoding of CC/MC, SD/S Frames with Time Tag
- Monitor Trigger on Command, SD/S Frame, ADW and DSI
- EFEX Transfer Error Detection
- Monitor Trigger on HS Frame Bus Errors
- EFEX Bus Recording and Replay at full Bus Rates

EFEX Bus Analyzer Software
AIM provides bus analyzer software specially extended to support EFEX data bus testing applications offered as
► **PBA.pro™** test and analysis tool (for Windows and Linux).



Physical Bus Replay

The APXX3910 module can reconstruct previously recorded ► **STANAG3910/EFEX** data bus traffic to both the LS electrical and HS optical databus simultaneously with excellent timing accuracy.
Recorded data files can be selected for physical bus replay.
The additional capability to disable any or all RT responses from the STANAG3910 replay enables smart systems integration and test to be performed.

Application Support Processor

The onboard Application Support Processor (ASP) section of the APXX3910 offers processing functions typically provided by the host processor system.

Operational features include:
- Driver Software Execution Onboard
- Dynamic Data Generation
- Runs under Linux Operating System

IRIG-B Time Encoder/Decoder

APXX3910 modules include an onboard IRIG-B time encoder/decoder with a sinusoidal output and a free-wheeling mode for time tag synchronization.
This allows synchronization of multiple APXX3910 or other AIM cards to 1 common IRIG-B time input source or to the onboard time code generator of 1 APXX3910 card as the reference for the correlation of data across multiple STANAG3910/EFEX streams.

Physical Bus Interface

The Physical Bus Interface (PBI) including Fibre Optic Front End (FOFE) and Dual Redundant STANAG3838/MIL-STD-1553B Transceiver (TRAFO) is implemented completely on a single board.

Bus Interface Unit (BIU) processors support the encoder/decoder functions for STANAG3910/EFEX and STANAG3838/ MIL-STD-1553A/B protocols.

The APXX3910 main board also supports both High Speed (HS) and MIL-STD-1553B Low Speed (LS) bus connections including a resistive terminated bus network as well as I/O connections for front panel triggering and IRIG-B signals.
Coupling to an external data bus system is software programmable.

Trigger-/General Purpose Discrete I/O Signals

The APXX3910 provides BC and BM trigger inputs, BC and BM trigger outputs and 8 user programmable General Purpose Discrete I/O signals (3 on front I/O, 8 on board-to-board connector).
Voltage levels of all trigger signals and General Purpose Discrete I/O's are TTL compatible whereby the General Purpose Discrete I/O's are designed to handle avionics level as well.

Driver Software Support

The driver software resides on the APXX3910 module. A full function Application Programming Interface (API) is provided compatible with Windows and Linux.

Host applications can be written in C++, LabWindows/CVI etc.
A LabView/VI application interface is provided as well.

Technical Data

Sub-System Interface
5V tolerant PCI-Bus Master and Slave, compliant with PCI-Standard V3.0 (32-bit, 33/66MHz)

Processors
System-on-Chip Device with 2 Dual Core Processing sections operated at up to 1200MHz

Memory
1GB LPDDR4 RAM

Encoder/Decoder
STANAG3910/STANAG3838 with full error injection and detection capability

Time Tagging
46-bit absolute IRIG-B time with 1µs resolution, sinusoidal IRIG-B output with free-wheeling mode

Trigger I/O
BC and BM trigger input, BC and BM trigger output for LS-Bus, BM trigger output for HS-Bus (all TTL compatible)

Discrete I/O
8 Open/Ground Avionics Level (+35V) discrete I/O

Physical Bus Interface (PBI)
Physical Bus Interface (PBI) including Fibre Optic Front End and Dual Redundant STANAG3838/MIL-STD-1553B Transceiver (TRAFO) with variable output amplitude, programmable bus coupling modes with onboard terminated bus network

Connectors
2 HA06-N aircraft style Fibre Optic connectors with normal orientation and STANAG3838/MIL-STD-1553B connections via high density D-Sub 15 way connector including TTL-trigger I/O, IRIG-B time code I/O signals, 3x discrete I/O's, 16-pin ribbon cable (board-to-board) connector with 8x discrete I/O's

Dimensions
168mm x 107mm short length PCI format

Power Consumption
10W typical @5VDC supply

Operating Temperature Range
Standard 0°C to +45°C
Extended temperature range -15°C to +60°C

Storage Temperature Range
-40°C to +85°C

Humidity
0 to 95% non-condensing

Ordering Information

APXX3910
Single stream, dual redundant PCI bus to STANAG3910/EFEX interface:

BC, Multi RT Simulator with Mailbox and Chronological Monitor, IRIG-B time encoder/decoder, 8 general purpose discrete I/O's (3 on front I/O, 8 on board-to-board connector), 1GB LPDDR4 RAM, onboard FOFE modules with 2x EFAbus optical connectors

ACB3910-HD15:
Ready made adapter cable for high density D-Sub to 2x Twinax connectors PL-75 and 1x 15-pin D-Sub connector for IRIG-B and trigger I/O

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